

FIG. 6A

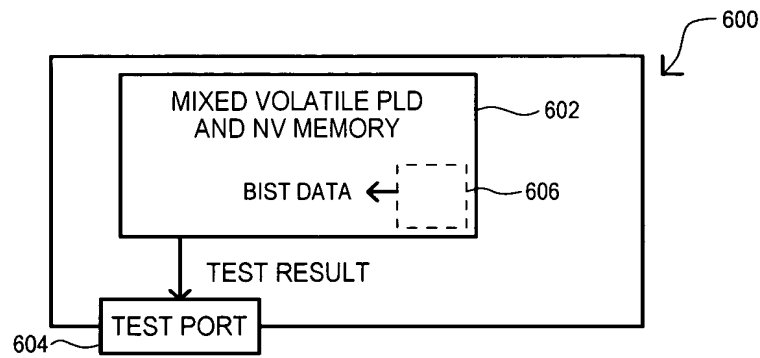


FIG. 6B

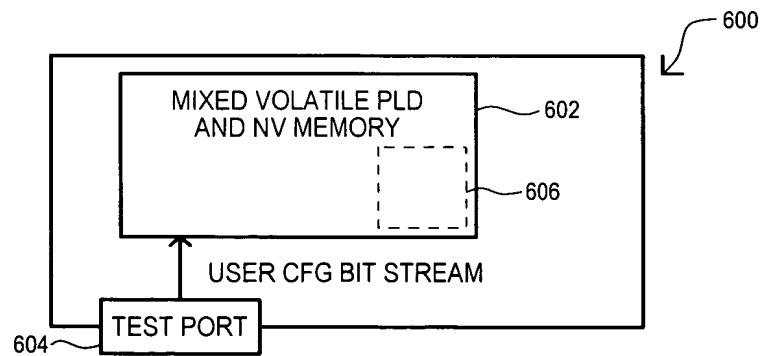


FIG. 6C

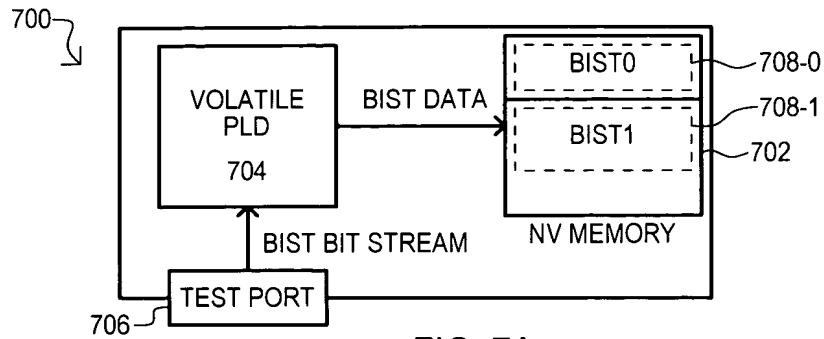


FIG. 7A

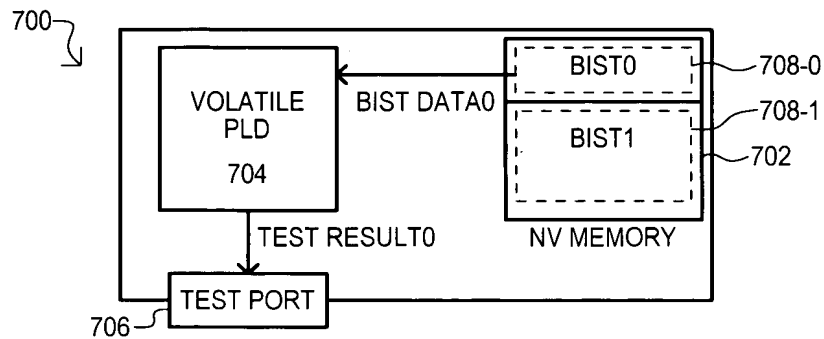


FIG. 7B

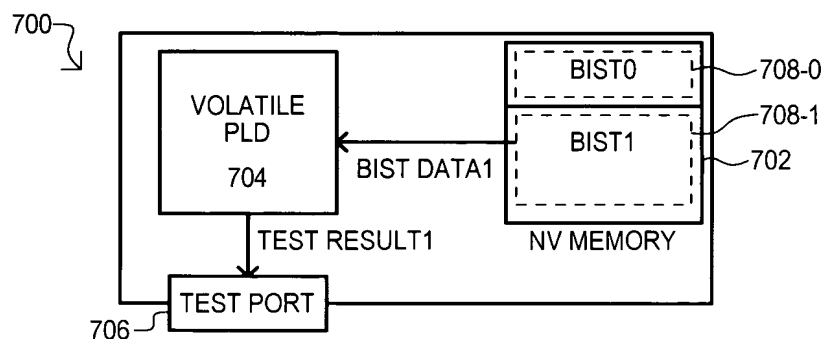


FIG. 7C

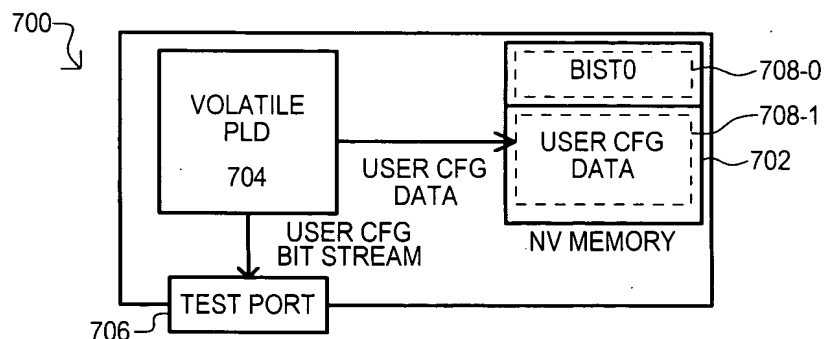


FIG. 7D

FIG. 8A is a block diagram of a device 800. The device 800 contains a VOLATILE PLD 804-0 and NV MEMORY 802. A TEST PORT 806 is connected to the VOLATILE PLD 804-0 via a TEST COMM line. A dashed line 804-1 is shown within the VOLATILE PLD 804-0.

FIG. 8B is a block diagram of a device 800. The device 800 contains a VOLATILE PLD 804-0, an NV MEMORY 802, and a TEST PORT 806. A dashed line 804-1 is shown within the VOLATILE PLD 804-0. The TEST PORT 806 is connected to the VOLATILE PLD 804-0 and the NV MEMORY 802. The TEST PORT 806 is also connected to the TEST RESULT output.

FIG. 8C

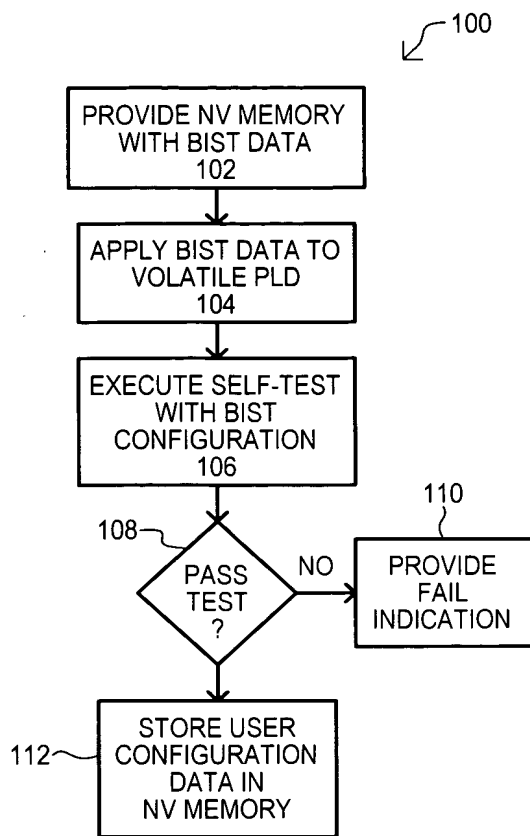
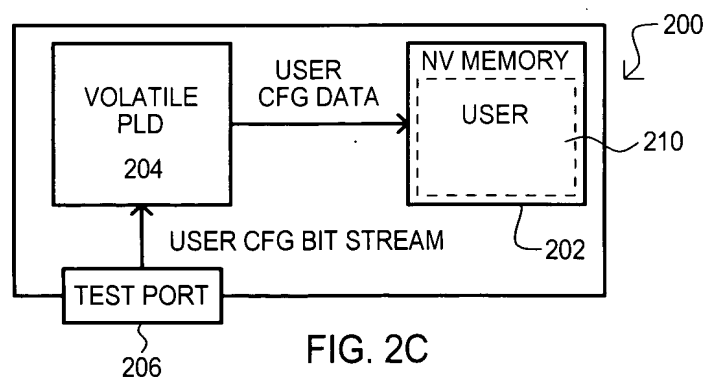


FIG. 1

FIG. 2A

FIG. 2B



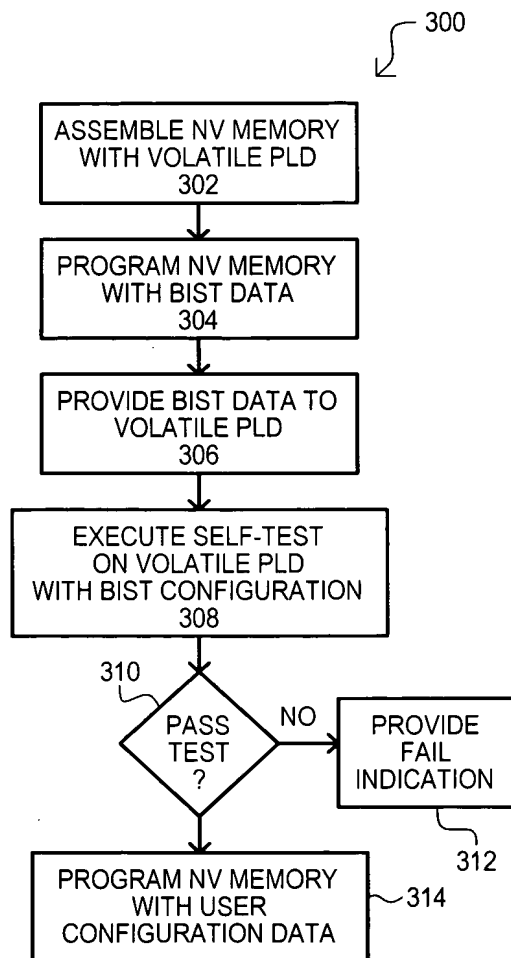
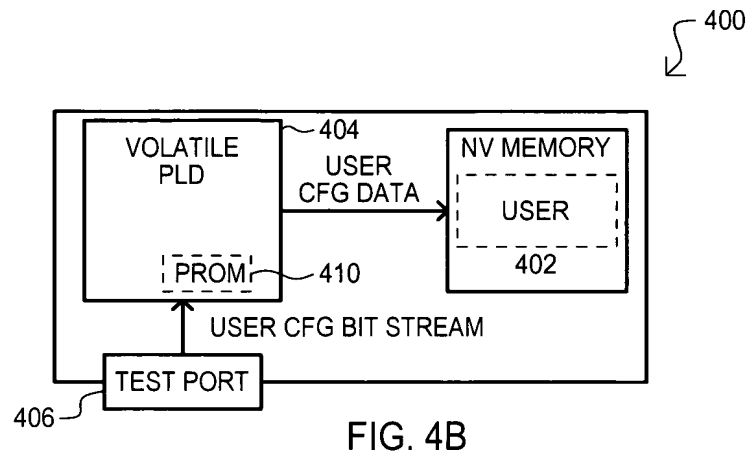
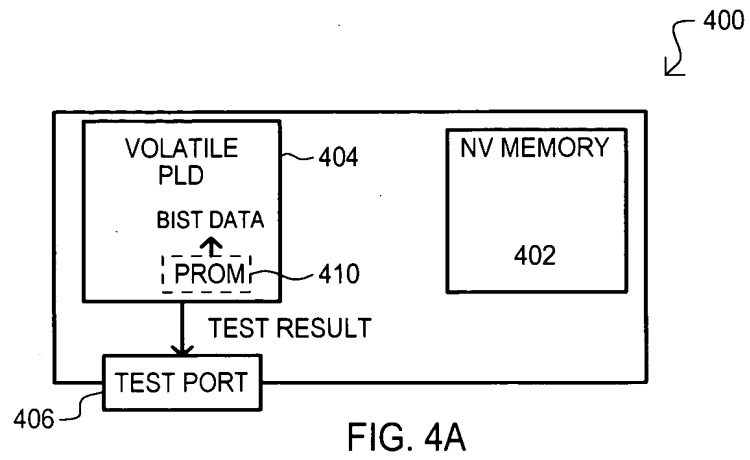


FIG. 3



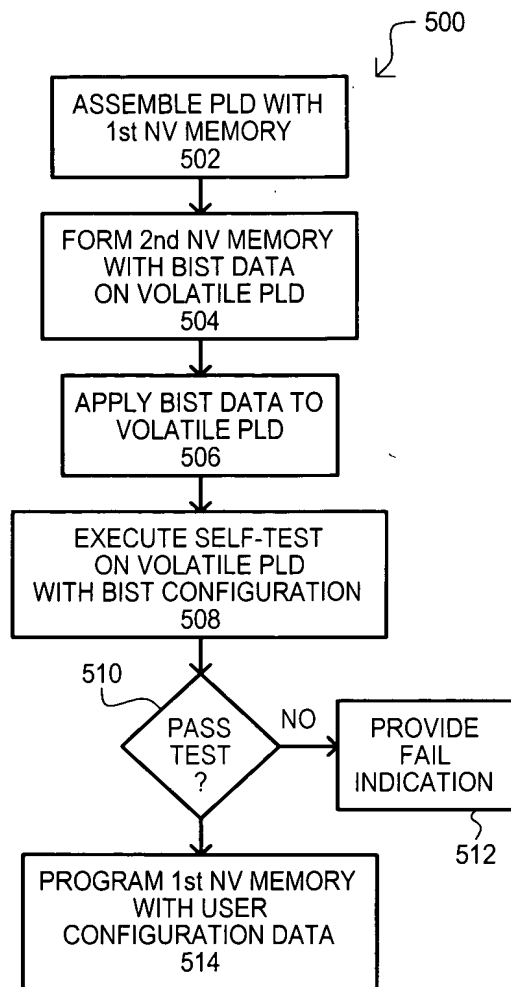


FIG. 5